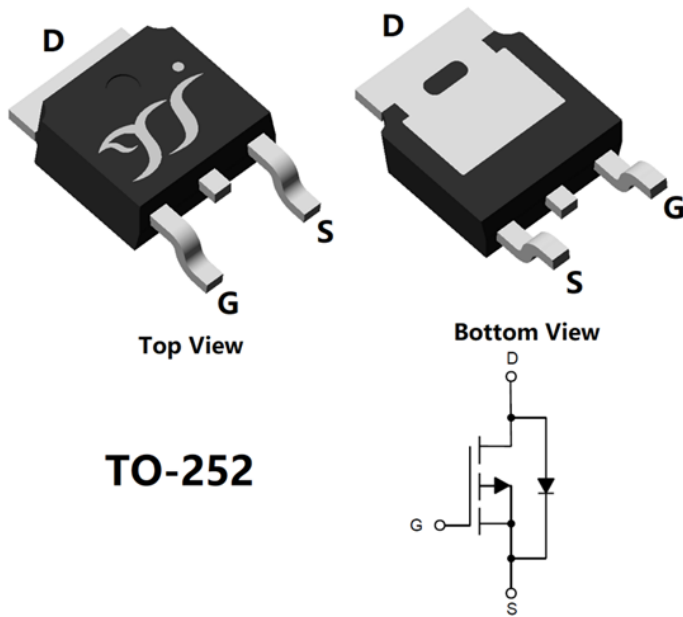




P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -60V
- I_D -60A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) $<15m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Fast Switching Speed
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Load Switch
- DC-DC convertor

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-60	V
Gate-source Voltage ^E		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	-9	A
	$T_A=100^\circ C$		-6	
	$T_C=25^\circ C$		-60	
	$T_C=100^\circ C$		-42	
Pulsed Drain Current ^A		I_{DM}	-200	A
Avalanche energy ^B		EAS	118.81	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	3	W
	$T_A=100^\circ C$		1.5	
	$T_C=25^\circ C$		100	
	$T_C=100^\circ C$		50	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+175	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.2	1.5	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD015GP06AHQ	F1/F2	YJD015GP06A	2500	/	25000	13"Reel



YJD015GP06AHQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-60	-	-	V
		V _{GS} = 0V, I _D =-1mA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-60V, V _{GS} =0V, T _j =125°C	-	-	-100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-1.5	-2.3	-3.1	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-30A	-	12	15	mΩ
Diode Forward Voltage	V _{SD}	I _S =-30A, V _{GS} =0V	-	-	-1.2	V
Gate resistance	R _G	f=1MHz	-	1.3	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-60	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, f=1MHz	-	3035	-	pF
Output Capacitance	C _{oss}		-	500	-	
Reverse Transfer Capacitance	C _{rss}		-	20	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-30A	-	52.6	-	nC
Gate-Source Charge	Q _{gs}		-	15.8	-	
Gate-Drain Charge	Q _{gd}		-	10.6	-	
Reverse Recovery Charge	Q _{rr}	I _F =-30A, di/dt=100A/us	-	80.5	-	nC
Reverse Recovery Time	t _{rr}		-	52.4	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-30V, I _D =-30A R _{GEN} =3Ω	-	21	-	ns
Turn-on Rise Time	t _r		-	88	-	
Turn-off Delay Time	t _{D(off)}		-	43	-	
Turn-off fall Time	t _f		-	95	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_G=-10V, R_G=25Ω, L=0.5mH, I_{AS}=-21.8A.

C. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on the 40mm*40mm*1.1mm FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.

E. V_{GS}=-20V/+10V according AEC-Q101 at T_J=175°C.



■ Typical Electrical and Thermal Characteristics Diagrams

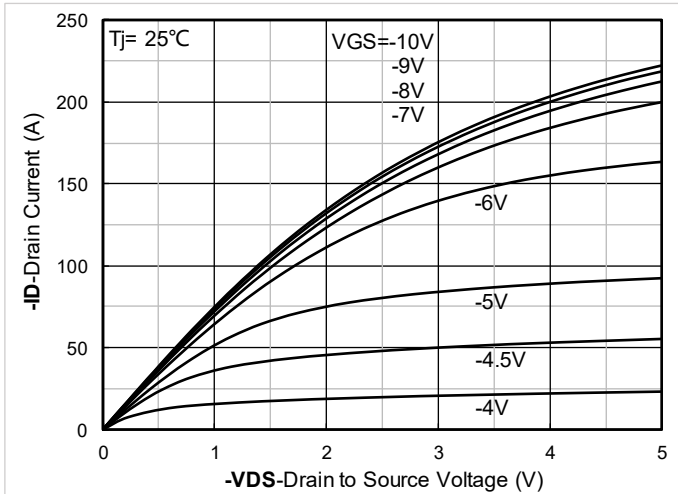


Figure 1. Output Characteristics

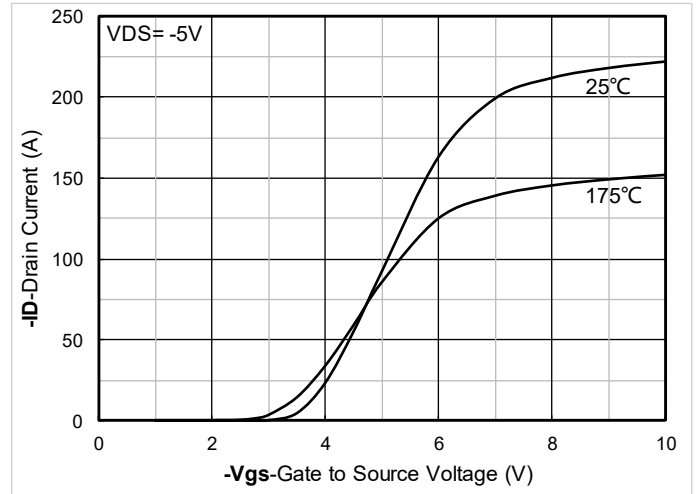


Figure 2. Transfer Characteristics

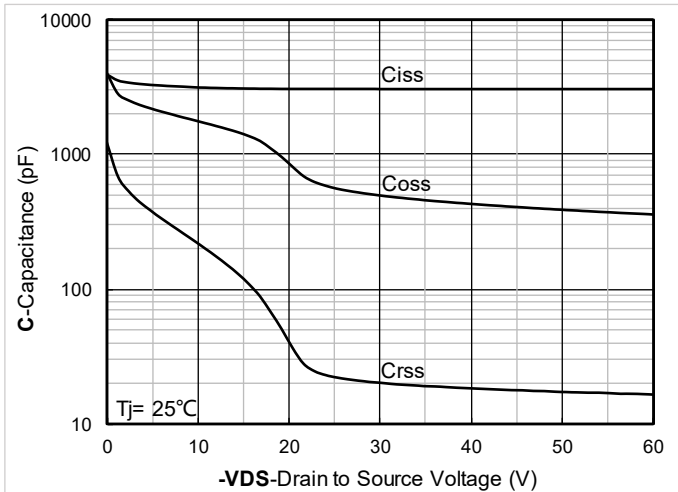


Figure 3. Capacitance Characteristics

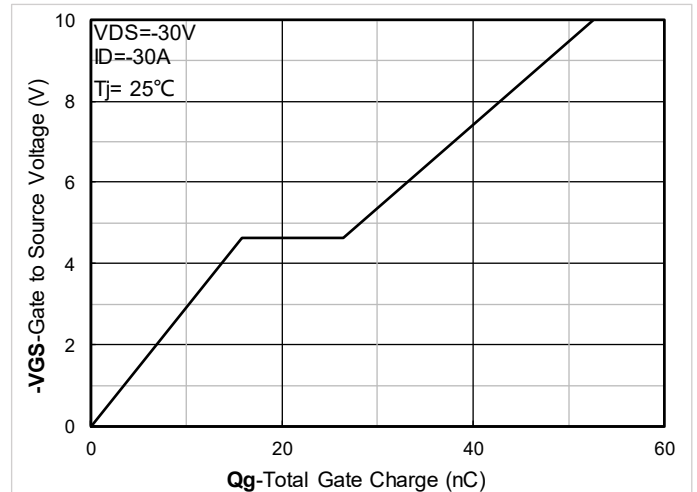


Figure 4. Gate Charge

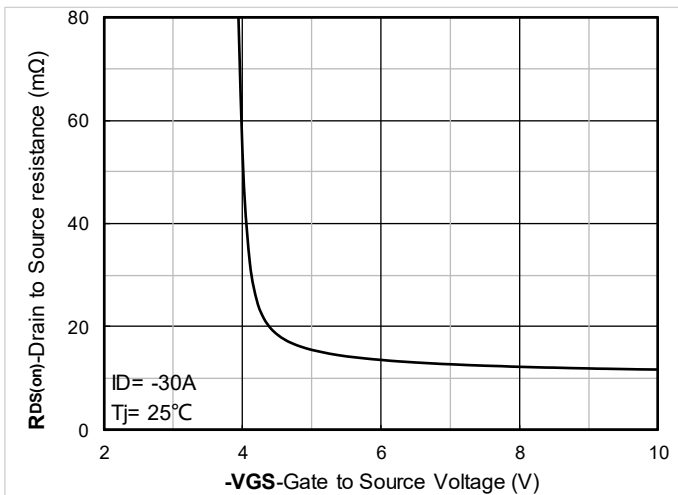


Figure 5. On-Resistance vs Gate to Source Voltage

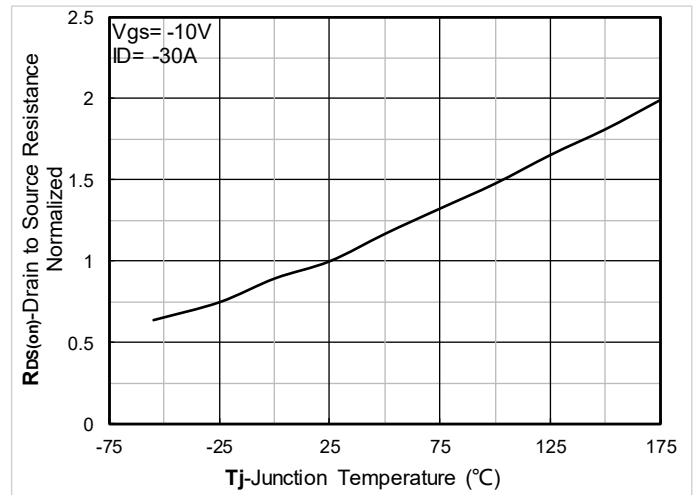


Figure 6. Normalized On-Resistance

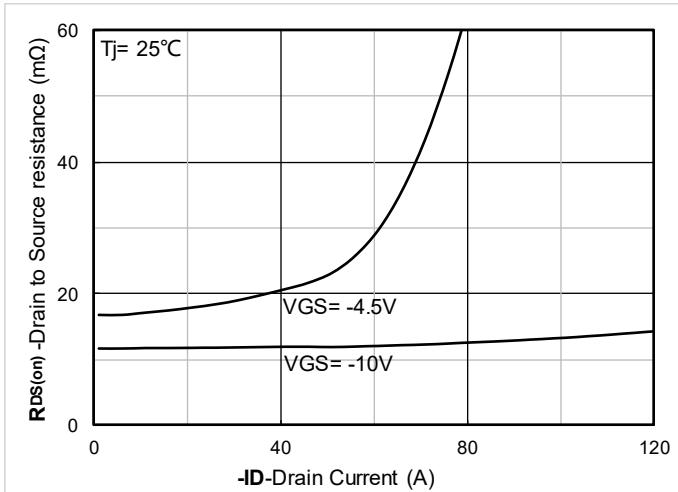


Figure 7. RDS(on) VS Drain Current

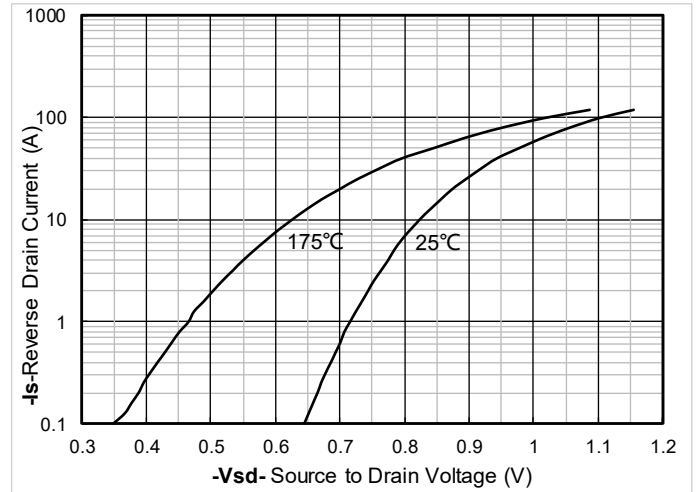


Figure 8. Forward characteristics of reverse diode

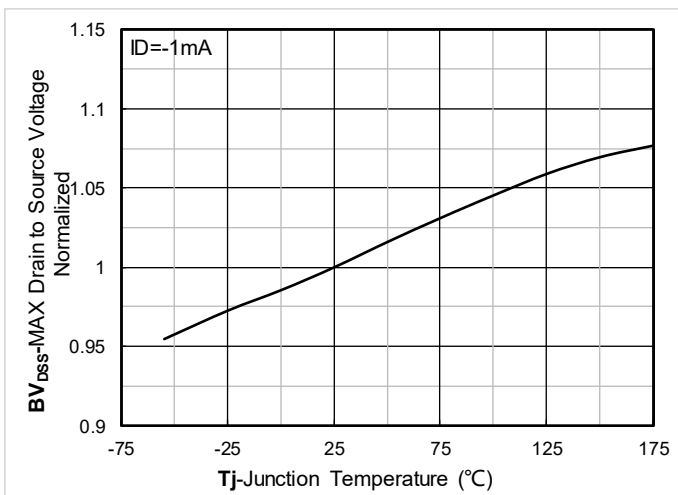


Figure 9. Normalized breakdown voltage

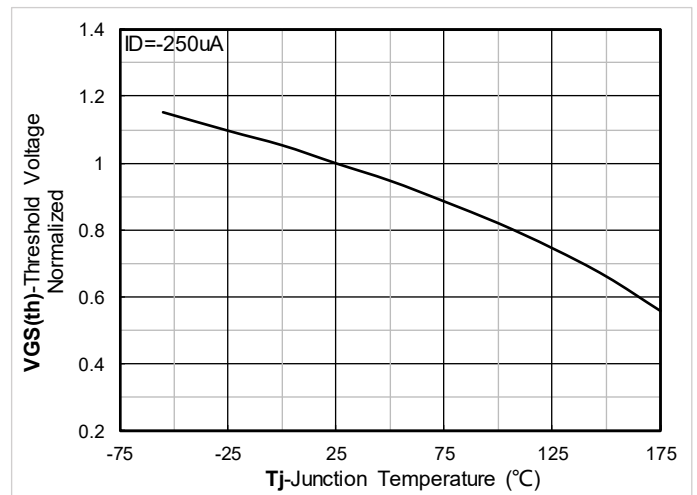


Figure 10. Normalized Threshold voltage

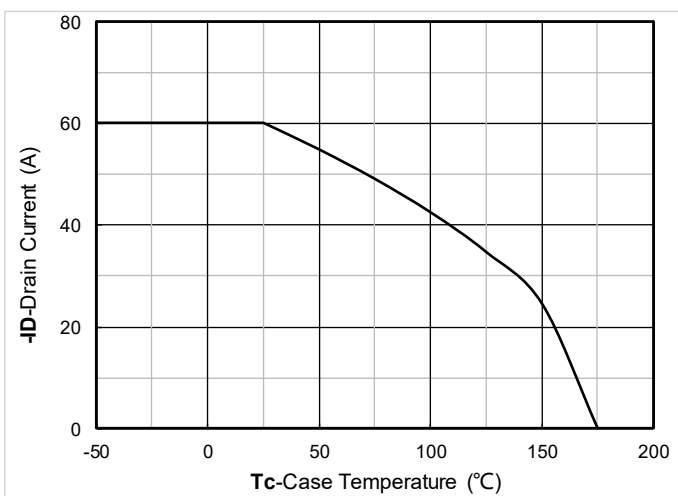


Figure 11. Current dissipation

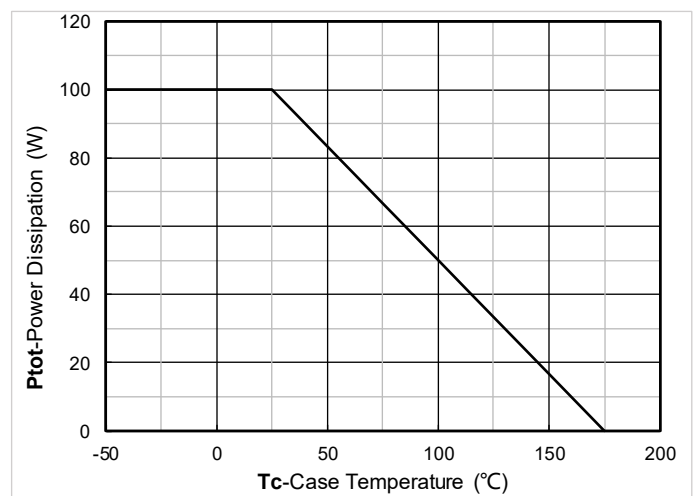


Figure 12. Power dissipation

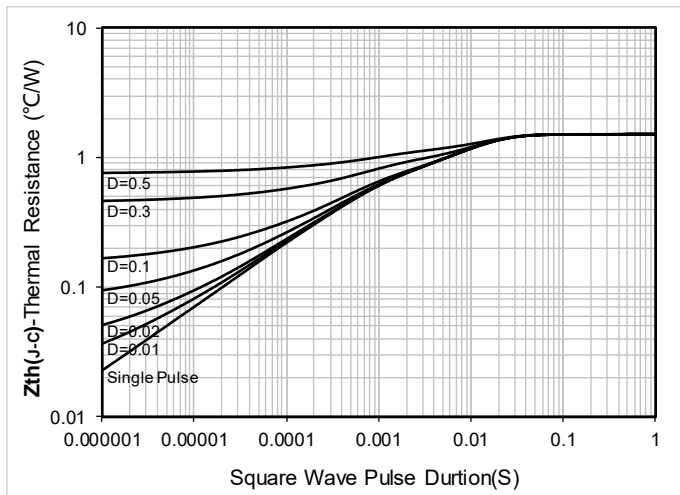


Figure 13. Maximum Transient Thermal Impedance

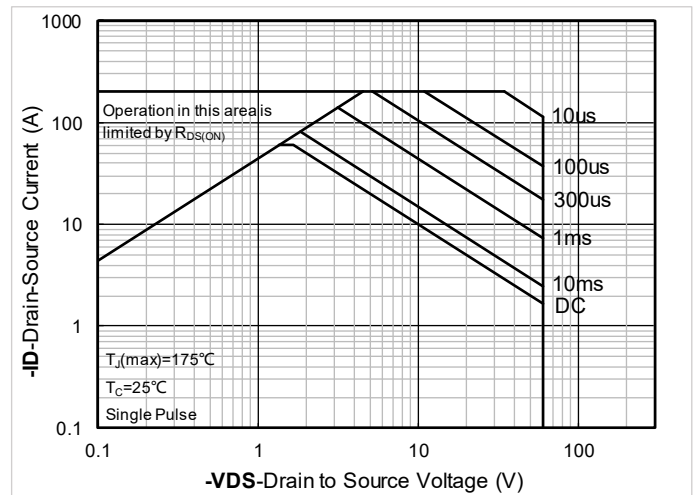
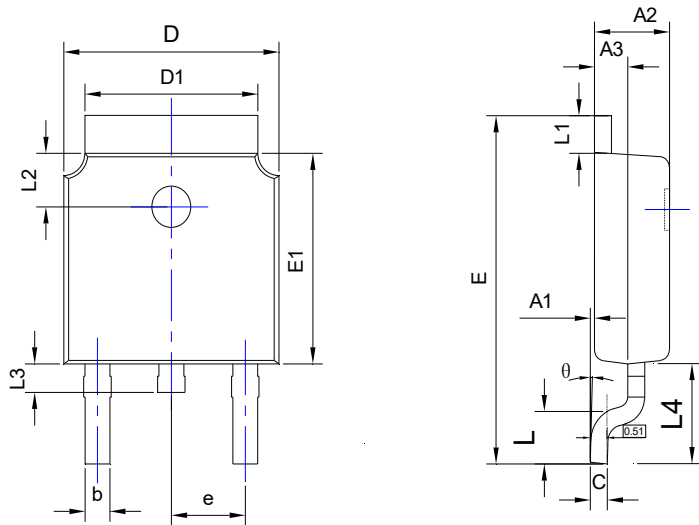


Figure 14. Safe Operation Area



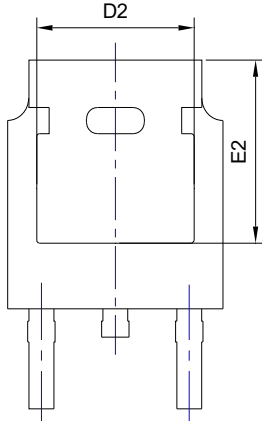
YJD015GP06AHQ

■ TO-252-B Package information

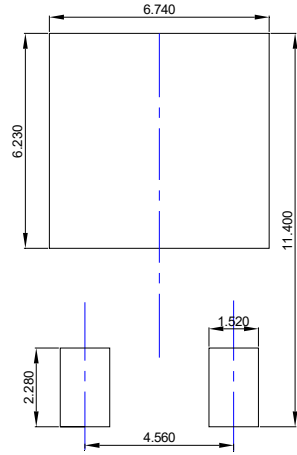


TOP VIEW

SIDE VIEW



BOTTOM VIEW



SUGGESTED SOLDER PAD LAYOUT

UNIT: mm

SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.024	0.031	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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